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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,524	10/25/2002	Chau-Chad Tsai	JCLA8269	2141
23900	7590	11/19/2004	EXAMINER	
J C PATENTS, INC. 4 VENTURE, SUITE 250 IRVINE, CA 92618			CLEARY, THOMAS J	
			ART UNIT	PAPER NUMBER
			2111	
DATE MAILED: 11/19/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/065,524

Applicant(s)

TSAI ET AL.

Examiner

Thomas J. Cleary

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 25 October 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) ^o
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 6,067,590 to Pettey et al. ("Pettey").

3. In reference to Claim 1, Pettey discloses a method of hot switching data transfer rate on the bus, to dynamically switch the bus data transfer rate between a first control chip (See Figure 1 Number 109) and a second control chip (See Figure 1 Number 130), comprising the steps of: the first control chip and the second control chip receiving a transfer rate switching command (See Column 11 Lines 1-6). The first control chip of Pettey will inherently issue a command equivalent to a bus release connect command when either there is no data transaction processed or the data transaction process is finished; the first control chip and the second control chip of Pettey will further inherently enter into the bus release connect state according to the bus release connect command. Pettey further discloses that the first control chip issues a bus re-connect

command (See Column 11 Lines 14-15); and the first control chip and the second control chip re-connecting to the changed data transfer rate according to the transfer rate switching command (See Column 11 Lines 12-19).

4. In reference to Claim 2, Pettey discloses the limitations as applied to Claim 1 above. Pettey further discloses that the first control chip is a north-bridge chip (See Figure 1 Number 109), and the second control chip is a south-bridge chip (See Figure 1 Number 130).

5. In reference to Claim 5, Pettey discloses a method of hot switching data transfer rate on the bus, comprising the steps of: a bus between a first control chip (See Figure 1 Number 109) and a second control chip (See Figure 1 Number 130) receiving a transfer rate switching signal before data transfer is interrupted (See Column 11 Lines 1-6); and when the first control chip and the second control chip are re-connecting, providing one of a plurality of data transfer rates to the bus according to the transfer rate switching signal (See Column 11 Lines 12-19).

6. In reference to Claim 6, Pettey discloses the limitations as applied to Claim 5 above. Pettey further discloses that the first control chip is a north-bridge chip (See Figure 1 Number 109), and the second control chip is a south-bridge chip (See Figure 1 Number 130).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pettey as applied to Claims 2 and 6 above, and further in view of US Patent Number 6,163,826 to Khan et al. ("Khan").

9. In reference to Claim 3, Pettey teaches the limitations as applied to Claim 2 above. Pettey further teaches that the data transfer rate is switched between 33 Mhz and 66 Mhz (See Column 10 Line 66 – Column 11 Line 18). Pettey does not teach that the data transfer rate is switched between four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency. Khan teaches a bus interface, which is equivalent to the north-bridge, that has a chip clock frequency of 8 Mhz (See Column 4 Lines 32-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the 8 Mhz interface of Khan, resulting in the invention of Claim 3, in order to provide efficient full-duplex and half-duplex bidirectional communications to peripheral devices (See Column 4 Lines 32-34).

10. In reference to Claim 7, Pettey teaches the limitations as applied to Claim 6 above. Pettey further teaches that the data transfer rate is switched between 33 Mhz and 66 Mhz (See Column 10 Line 66 – Column 11 Line 18). Pettey does not teach that the data transfer rate at least comprises four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency. Khan teaches a bus interface, which is equivalent to the north-bridge, that has a chip clock frequency of 8 Mhz (See Column 4 Lines 32-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the 8 Mhz interface of Khan, resulting in the invention of Claim 7, in order to provide efficient full-duplex and half-duplex bidirectional communications to peripheral devices (See Column 4 Lines 32-34).

11. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pettey as applied to Claims 1 and 5 above, and further in view of US Patent Number 6,507,879 to Sayles ("Sayles").

12. In reference to Claim 4, Pettey teaches the limitations as applied to Claim 1 above. Pettey does not teach that the first control chip and the second control chip both have a transfer rate register for temporarily storing the transfer rate switching command. Sayles teaches command registers in interconnected bus bridges for setting the transfer rate of communications (See Column 5 Lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the transfer rate command registers of Sayles, resulting in the invention of Claim 4, in order to provide an indication of which transfer mode is to be utilized for data transfers (See Column 6 Lines 59-61 of Sayles).

13. In reference to Claim 8, Pettey teaches the limitations as applied to Claim 5 above. Pettey does not teach that the first control chip and the second control chip both have a transfer rate register for temporarily storing the transfer rate switching command. Sayles teaches command registers in interconnected bus bridges for setting the transfer rate of communications (See Column 5 Lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the transfer rate command registers of Sayles, resulting in the invention of Claim 8, in order to provide an indication of which transfer mode is to be utilized for data transfers (See Column 6 Lines 59-61 of Sayles).

14. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pettey and Sayles.

15. In reference to Claim 9, Pettey teaches method of hot switching data transfer rate on the bus, to dynamically switch a plurality of data transfer rates on a bus between a

first control chip (See Figure 1 Number 109) and a second control chip (See Figure 1 Number 130), comprising the steps of: the first control chip and the second control chip receiving a data transfer rate switching command (See Column 11 Lines 1-6). The first control chip of Pettey will inherently issue a command equivalent to a bus release connect command when either there is no data transaction processed or the data transaction process is finished to have the first control chip and the second control chip enter into the bus release connect state. Pettey further teaches that the first control chip issues a bus re-connect command (See Column 11 Lines 14-15); and the first control chip and the second control chip re-connecting to the changed data transfer rate according to the transfer rate switching command (See Column 11 Lines 12-19). Pettey does not teach temporarily storing the data transfer rate switching command into a transfer rate register of the first control chip and the second control chip. Sayles teaches command registers in interconnected bus bridges for setting the transfer rate of communications (See Column 5 Lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the transfer rate command registers of Sayles, resulting in the invention of Claim 9, in order to provide an indication of which transfer mode is to be utilized for data transfers (See Column 6 Lines 59-61 of Sayles).

16. In reference to Claim 10, Pettey and Sayles teach the limitations as applied to Claim 9 above. Pettey further teaches that the first control chip is a north-bridge chip

(See Figure 1 Number 109), and the second control chip is a south-bridge chip (See Figure 1 Number 130).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the transfer rate command registers of Sayles, resulting in the invention of Claim 10, in order to provide an indication of which transfer mode is to be utilized for data transfers (See Column 6 Lines 59-61 of Sayles).

17. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pettey and Sayles as applied to Claim 10 above, and further in view of Khan.

18. In reference to Claim 11, Pettey teaches the limitations as applied to Claim 10 above. Pettey further teaches that the data transfer rate is switched between 33 Mhz and 66 Mhz (See Column 10 Line 66 – Column 11 Line 18). Pettey and Sayles do not teach that the data transfer rate at least comprises four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency. Khan teaches a bus interface, which is equivalent to the north-bridge, that has a chip clock frequency of 8 Mhz (See Column 4 Lines 32-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Pettey with the 8 Mhz interface of Khan, resulting in the invention of Claim 11, in order to provide efficient full-duplex and half-duplex bidirectional communications to peripheral devices (See Column 4 Lines 32-34).

Conclusion

The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US Patent Number 5,758,133 to Evoy; US Patent Number 5,935,232 to Lambrecht et al.; US Patent Number 6,539,443 to Dunstan et al.; US Patent Number 6,732,190 to Williams et al.; and US Patent Application Publication Number 2002/0171456 to Solomon.

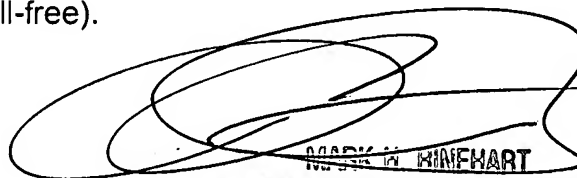
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

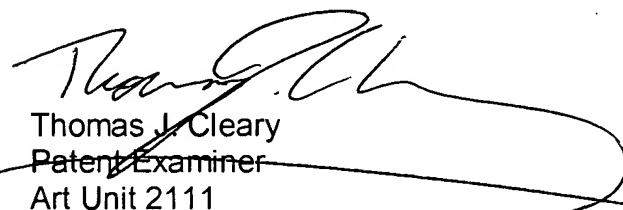
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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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